

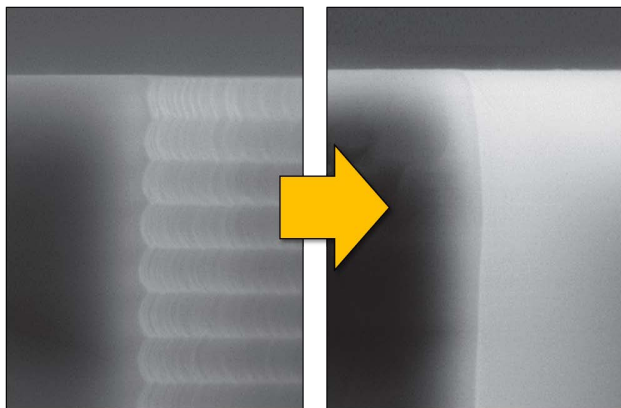
### Introduction

DRIE silicon etching is a key technology for MEMS device production. The process uses sequential isotropic etch and passivation steps to produce a highly anisotropic etch ideal for the formation of high aspect-ratio features. As a consequence, the sidewalls of features etched by DRIE feature multiple indentations called scallops.

For some MEMS devices scalloped sidewalls are undesirable as they can be a source of electro-static or mechanical stiction. In addition, the sharp corners of DRIE etched features can concentrate stresses which may cause mechanical failures. In these cases, a thermal anneal can be employed to transform the Si surface.

### Si Transformation Anneal

Surface transformation is achieved by annealing the Si wafers at high temperature (~1100°C) in a H<sub>2</sub> ambient. Under these conditions, the mobility of the Si atoms at the surface is increased and the scallops are eliminated by the mass transit effect. This effect also transforms sharp corners into rounded features.



Scallop elimination via H<sub>2</sub> annealing

### Rapid Vertical Processor

The H<sub>2</sub> anneal process can be performed in SPT's RVP vertical furnace configured with Advanced Temperature Control (ATC). This platform ensures the highest productivity by minimizing the heating and cooling time while ensuring that the mechanical stability of the wafers is maintained by avoiding the formation of slip dislocations in the Si lattice.



### RVP H<sub>2</sub> Anneal Benefits

Key benefits of using SPT's H<sub>2</sub> annealing process:

- >3x lower cost and smaller footprint vs. competing single-wafer solutions
- Low O<sub>2</sub> environment to prevent native oxidation and ensure process safety
- Uniform processing over 100-wafer batch
- Run 150mm and 200 mm wafers simultaneously with no hardware changes
- Compatible with perforated, bonded and thin substrates

### Certified for Safety

SPT's high temperature RVP furnace has been fully evaluated for H<sub>2</sub> annealing safety by certified 3<sup>rd</sup> parties.