SPTS
A KLA Company

APPLICATION
BRIEF

Blanket Silicon Etching

Introduction

When it comes to patterned silicon etching a commonly accepted trend is towards smaller features and higher aspect ratios. However, blanket Si etches are still required across some traditional and a growing number of emerging markets.

Examples of dry blanket etching include:

- Stress relief following mechanical grinding for thin wafers used in power semiconductors
- Removing over-hangs introduced during tapered trench or via etching to aid deposition into TSVs for CMOS image sensor packaging
- Removing the Si wafer from the active GaN and related layers of LEDs
- Via reveal etches that expose TSVs from the backside of the wafer for subsequent CVD, CMP and RDL metallization

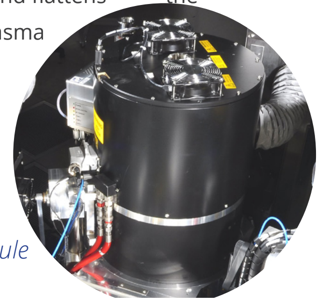
Why Use Plasma Etch

Compared to wet chemical approaches dry blanket Si etching exhibits better control over the etch rate and uniformity and has the benefit of being non-crystallographic.

All of the applications listed above require the best possible etch uniformity in combination with a productive etch rate. The last 2 applications also require etch selectivity, either to compound layers or to the TSV liner oxide. Via reveal etching is normally carried out on 300mm wafers but the other applications still remain at ≤200mm wafer size.

DSi-v for 200mm

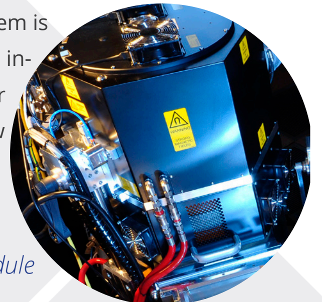
SPTS has developed blanket Si etches on all common wafer sizes. The Rapier™ process module is well suited to Bosch etching but it is the DSi-v module that offers a more productive fit for blanket etching on ≤200mm wafers. The unique design of the DSi-v enhances etch rate and flattens the uniformity profile through the use of plasma confinement hardware. Throughput is increased through the use of SF_6 chemistry and no inter-wafer cleans.



DSi-v silicon etch module

Rapier™ XE for 300mm

In the case of 300mm blanket etching for via reveal applications, however, the Rapier™ XE delivers the industry's most productive process through the use of a patented dual source technology with independent primary and secondary source powers and gas introduction. The Rapier™ XE has demonstrated etch rates >9μm/min with 200:1 selectivity to the oxide liner, surface roughness ≤1nm (Ra) and ≤±3% uniformity on 300mm wafers with 3mm edge exclusion. This enhanced Rapier™ system is also available with ReVia®, SPTS' unique in-situ endpoint solution, that can monitor the via reveal process for extremely low (0.01%) via density and extremely low reveal heights (~1μm).



Rapier™ XE silicon etch module

SPTS Technologies, a KLA company, designs, manufactures, sells, and supports etch, PVD, CVD and MVD® wafer processing solutions for the MEMS and sensors, advanced packaging, photonics, high speed RF, and power device markets. For more information, email enquiries@spts.com or visit www.spts.com

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