SPTS
A KLA Company

APPLICATION
BRIEF

Back-side Metal PVD for Power

Introduction

Power devices are semiconductor devices used as a switch or rectifier in power electronics. They are used for a wide range of applications from consumer goods such as washing machines, refrigerators, cordless drills to electric vehicles (EVs), industrial motor control and renewable energy.

In a discrete power device, current flows through the silicon. Electrical contacts are made on both the front and back-side of the die.

To make the back-side connection, after front-side processing is complete, wafers are thinned (to improve electrical performance, or 'on-state' resistance), and turned upside down for metal contact layers to be deposited using physical vapor deposition.

Back-side Metal Process Steps

There are several metal layers deposited in back-side metallization (BSM), along with pre-treatment steps beforehand to ensure good quality metal is produced with good adhesion, electrical properties and long-term reliability.

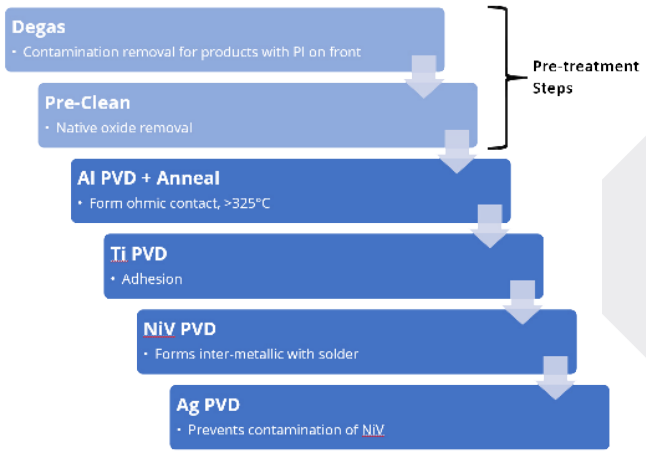


Fig. 1 Illustrates individual BSM process steps, common metals used, and their purpose

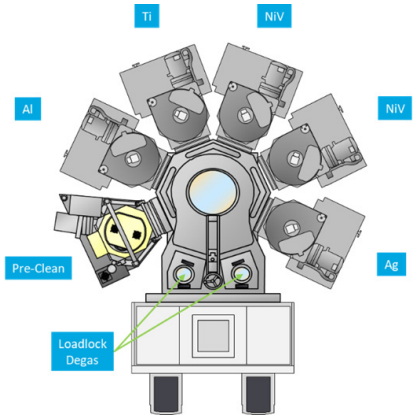


Fig. 2 Example of 300mm Sigma® fxP for back-side metallization

Edge Contact Wafer Handling

With trends towards thinner wafers for improved performance, wafer bow becomes increasingly challenging from a handling perspective. If carriers or protective tapes are not used then the active front-side of the wafer (which is face-down during back-side processing) must not touch any chamber hardware. SPTS's Sigma® *fx*P includes optional *edge contact* handling, where only the outer edge of the wafer is supported. This option, together with modified robot velocities, enables reliable handling of thinned, bowed and TAIKO wafers, without damaging the front-side of the wafer.

Importance of Degas

With any PVD process it is important to remove contamination from wafers prior to deposition. Outgassing during deposition can contaminate films, adversely impacting film properties and adhesion. Historically, power devices were fabricated using materials that did not adsorb contaminants, but more recently manufacturers have adopted organic-based materials such a polyimide (PI) instead of, or in addition to, PECVD SiN that was traditionally used for passivation. PI is known to absorb moisture in air, so removal of this contaminant prior to deposition is important, particularly with 300mm wafers where the volume of organic material on the wafer is larger.

For ultra-thin silicon wafers, where the substrate is mounted on a rigid carrier such as glass or silicon, bonding adhesives are used which compound the problem, resulting in a need for an even more thorough degas. For organic passivation cases, a lamp-based degas in the single wafer loadlock within the transport module (shown in Fig. 3a) is usually sufficient, but for bonded wafers, SPTS's multi-wafer degas (MWD) technology (Fig 3b) can offer effective, high vacuum degas capabilities *and* significant throughput advantages.

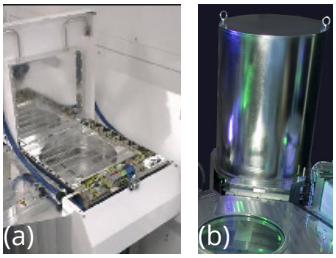


Fig. 3
(a) Lamp Degas Station (b) MWD

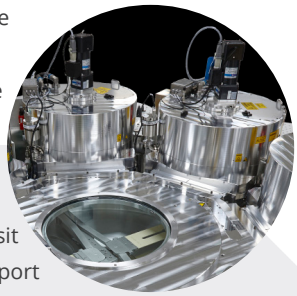
Low Damage Pre-Clean Etch

In order to make good electrical contact to the back of the silicon and achieve good adhesion for successful integration and long-term reliability, wafers require a pre-clean step after degas to remove and native oxide on the back-side Si. This can be achieved using an off-line wet HF dip, or in-situ, on the PVD system in a dedicated etch module. In-situ etching has the advantage of eliminating queue time constraints.

Historically, Ar sputter etch technology has been used for the pre-clean step, but to mimimize damage to the Si lattice, 'reactive' etch processes are often used. SPTS's Reactive Hot Soft Etch (RHSE) module is an inductively coupled plasma (ICP) source using a H_2 plasma to chemically remove native oxide, avoiding the high energy ion bombardment of an Ar sputter etch.

Optimization of BSM Layers

The materials used for the back-side metal stacks vary depending on the device type and the solder used for the subsequent assembly stage, but the most common are Ti-NiV-Ag for FETs, and for some devices (mainly IGBT), a thin layer of Al or Al alloy is deposited prior to the Ti-NiV-Ag stack.



Conventional PVD modules are used to deposit the layers but with additional features to support thin wafer back-side processing such as *edge contact* mentioned above, and *shadow shielding* to prevent metal overspill.

In-situ Al Anneal

After deposition, the Al is annealed to form a low resistive ohmic contact between the Si and the Al. A temperature of >325°C is required for this reaction to take place. Some device manufacturers remove wafers after Al deposition and anneal them in a dedicated furnace, before returning to a PVD system for the remaining materials in the BSM stack. To simplify the manufacturing process, the anneal can be performed within the PVD system. One approach is to cumulatively add heat into the wafer as it continues on its journey around the system after Al deposition, but this has the disadvantage that it relies on consistent, repeatable wafer scheduling and chamber pump recovery performance between wafers to ensure optimal wafer-to-wafer repeatability. It also limits stress control options for subsequent metals where temperature reduction is usually employed. Another approach is to send the wafer to an anneal station, or even back to a loadlock for a lamp-based anneal, which reduces throughput.

The Sigma® *fx*P performs the Al anneal in-situ, in the Al deposition chamber itself, avoiding any of the scheduling or vacuum recovery concerns from alternative approaches. Evidence of successful ohmic contact can be observed by removing the Al layer post-deposition using a wet etchant and inspecting the surface of the silicon. Regular pyramidal divets in the silicon (shown in Fig 4) indicates successful inter-diffusion between the Al and the Si, forming the desired low-resistive contact.

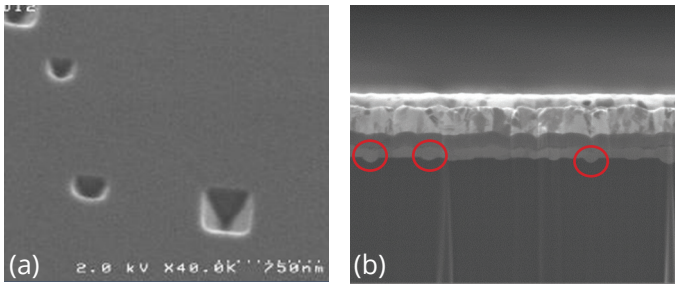


Fig. 4 (a) Pyramidal features indicative of Si junction spiking
(b) Cross-section of Al-Ti-NiV-Ag stack showing Al-Si inter-diffusion

Stress Control

Following deposition of the Al layer, PVD of the remaining layers is performed as cold as possible, to minimize extrinsic stress and subsequent warpage. SPTS use a *backfill cool* technique to remove heat from the wafers, either as they arrive from a previous hot process, or during the deposition. The *backfill cool* technique is a *non-clamped* approach that involves increasing chamber pressure to a level that will conduct heat away from the wafer to a chilled platen beneath, before opening up vacuum valves and initiating the sputter deposition process.

In addition to the *backfill cool* technique, pulsed DC, N_2 addition and traditional pressure adjustment can be used to control film stress. Having multiple stress control parameters allows the Sigma® to tune wafer bow. In some cases, wafers with larger incoming bow can emerge from the system effectively flat – ideal for processing further down the line.

For thin Si mounted on carriers, wafers will be flat, and more robust, so the use of *cold eectrostatic chuck* (ESC) technology is then an option to remove heat from the wafers more efficiently, increasing throughput.

SPTS Technologies, a KLA company, designs, manufactures, sells, and supports etch, PVD, CVD and MVD® wafer processing solutions for the MEMS, advanced packaging, LED, high speed RF, and power device markets. For more information about SPTS Technologies, email enquiries@spts.com or visit www.spts.com