SPTS
A KLA Company

CASE
STUDY

Blanket Silicon Etch for Lower Cost TSV

Customer

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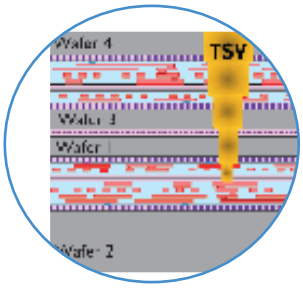
Application

Thinning wafers reduces the cost and technical difficulty of etching through-silicon vias (TSVs) in advanced "3D" packaging schemes. This case study discusses a joint development project between imec, SPTS and other partners to optimize a manufacturable "TSV-last" route for a multi-wafer stack using dielectric bonding and TSV interconnections.



Background

For a number of years, "3D packaging" has been promoted as the ideal way to continue improving in the Power Performance, Area and Cost (PPAC) trend in microelectronics and nanoelectronics, when the current industry strategy of simply reducing transistor gate width reaches its physical limitation. 3D packaging involves stacking chips and creating electrical connections between the different layers by etching TSVs and filling them with metal. To minimize the package size, there is the drive to make the diameter of TSV as small as possible, but this increases the *aspect ratio* of the etched via hole, unless the wafer thickness is reduced correspondingly. A narrow, high aspect ratio via hole is much slower to etch and therefore more expensive in production. Thinning a wafer by dry plasma etching alone can also be very slow and expensive, thus the majority of the silicon is removed by grinding down to 50µm. The surface is then smoothed chemical using mechanical polishing (CMP) which removes around 1µm of the remaining silicon, prior to a plasma-based blanket silicon etch to complete the thinning to the desired final thickness of around 5µm of remaining silicon. The thickness of the thinned wafer must be uniform across the whole wafer to ensure the subsequent dielectric bonding and TSV formation steps are successful.

OBJECTIVE

- Reduce cost of wafer thinning prior to TSV etch
- Reduce wafer thickness to 5µm
- Overcome in-coming thickness variation from grinding/CMP
- Improve cross-wafer thickness uniformity to ensure TSV connection
- Minimize edge "shamfer" to improve direct bonding step

SOLUTION

- Improved plasma source
- End-point detection for accurate depth control stopping on 5µm silicon

RESULTS

- Cost of wafer level processing by replacing 25µm of grinding and 19µm of CMP with 44µm plasma etch reduced by an estimated 50%[1]
- High Si etch rate >9µm/min
- Total Thickness Variation after plasma etching ~1.2µm (with an edge exclusion of 2mm)

[1] A. Jourdain et al., Extreme wafer thinning optimization for via-last applications", A. Jourdain et al., IEEE International Conference on 3D System Integration - 3DIC, San Francisco, CA, 2016

"*We have worked closely with SPTS for several years, on many aspects of advanced packaging and other areas of microelectronic manufacturing, and the development of this extreme thinning capability has a real potential to significantly reduce the cost of via-last 3D packaging.*" Eric Beyne, 3D Program Director and Fellow, imec.

SPTS Technologies, A KLA company, designs, manufactures, sells, and supports etch, PVD, CVD and MVD® wafer processing solutions for the MEMS, advanced packaging, LED, high speed RF on GaAs, and power management device markets. For more information about SPTS Technologies, email enquiries@spts.com or visit www.spts.com