SPTS
A KLA Company

CASE STUDY

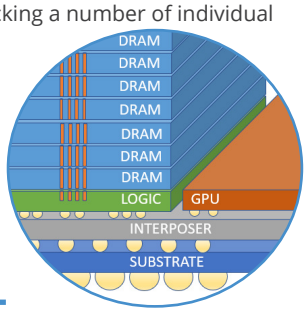
Via Reveal for High Bandwidth Memory

Customer

SK Hynix is a global semiconductor solution provider that mainly manufactures memory semiconductor products such as DRAM, NAND Flash and MCP (Multi-chip Package), with expansion into non-memory business through production of other products such as CMOS Image Sensors.
See **www.skhynix.com**

Application

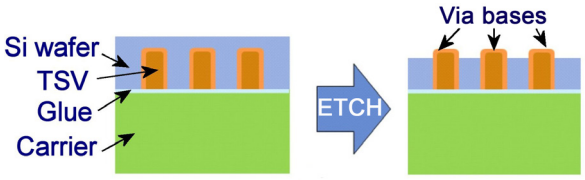
High bandwidth memory chips increase their speed and capacity while reducing power consumption, by stacking a number of individual DRAM die on top of each other and connecting them using through silicon via (TSVs), interposers and microbumps.



Background

In August 2019, SK Hynix launched their HBM2E DRAM chip which supports over 460GB per second bandwidth based on the 3.6Gbps speed performance per pin with 1,024 data I/Os. Using TSV technology, a maximum of eight 16-gigabit chips are vertically stacked, forming a single, dense package of 16GB data capacity. It is aimed at high-end machine learning, supercomputers and 5G network applications in the fourth industrial era.

Via Reveal Processing is an etch process which removes silicon from the backside of a wafer, until the bases of any TSVs within the wafer are revealed. Key challenges include achieving a high etch rate for a large exposed area, maintaining a uniform etch rate across the whole wafer, and real-time monitoring of the point at which the vias are revealed using automated end-point technology. It may also be necessary to adjust etch rate uniformity to compensate for variations in pre-etch silicon thickness across each wafer, and from one wafer to the next. Our Rapier™ XE utilizes a dual plasma source with multi-mode operation which allows for uniformity tuning that can compensate for incoming wafer thickness variations. Our unique ReVia® end-point technology provides in-situ monitoring of the via reveal process for any TSV layout or area.



Via Reveal Process

OBJECTIVE

- Increase productivity of backside via reveal process
- Optimize production yield
- Reduce cost of ownership

SOLUTION

- SPTS Omega® Rapier™ XE with ReVia® end-point detection was selected after a 9-month evaluation, compared against other plasma systems and wet etch options.

RESULTS

- The Rapier™ XE offered 2X the etch rate of competing plasma etch systems with reliable processing due to ReVia® EPD.
- System moved to high volume production line as new process of record for the via reveal step.

SPTS Technologies, A KLA company, designs, manufactures, sells, and supports etch, PVD, CVD and MVD® wafer processing solutions for the MEMS, advanced packaging, LED, high speed RF on GaAs, and power management device markets. For more information about SPTS Technologies, email enquiries@spts.com or visit www.spts.com