SPTS
A KLA Company

APPLICATION
BRIEF

Plasma Dicing

Introduction

Wafer dicing is generally carried out using conventional blade technology. However this method has limitations which can be overcome by using dry plasma etching.

Blade cutting can cause die chipping or cracking leading to lower device yields. Also the necessary width of the blade removes valuable "real estate" from the wafer. Deep Reactive Ion Etching (DRIE) is a dry plasma process which can etch very narrow, deep vertical trenches into silicon (known as dicing "streets") to separate individual die

Why Use Plasma Dicing?

- All dicing streets are etched simultaneously, resulting in throughputs at least 2 times greater than mechanical sawing
- Unlike sawing, plasma dicing will not damage the wafer surface or affect trench sidewall, resulting in greater die strengths, improved device reliability and increased device lifetime
- The narrower street widths of plasma dicing free up valuable wafer real estate allowing for increased die count on each wafer
- Non-rectangular die shapes can also be created (i.e. defined by mask, not blade cut) - see Fig 5 overleaf

Dicing Before Grind (DBG)

In the DBG approach, die are defined by partially etching the front side of a masked wafer up to a depth of approx 200µm. The wafer is then attached face-down to a dicing frame and the backside of the wafer ground away until singulation of the die occurs. Plasma dicing offers reduced cycle times and lower manufacturing costs when compared to conventional mechanical dicing.

SPTS's Mosaic™ Rapier-S DRIE systems provide 2 times greater throughputs than mechanical sawing, and have already been qualified at customer sites for this application.

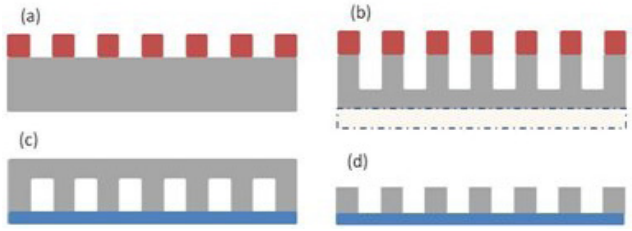

Fig 1 Schematic diagram illustrating Dicing Before Grind

Dicing After Grind (DAG)

In the case of DAG, device wafers are thinned, then taped onto frames. The die are then singulated by etching through the complete silicon thickness, to the tape.

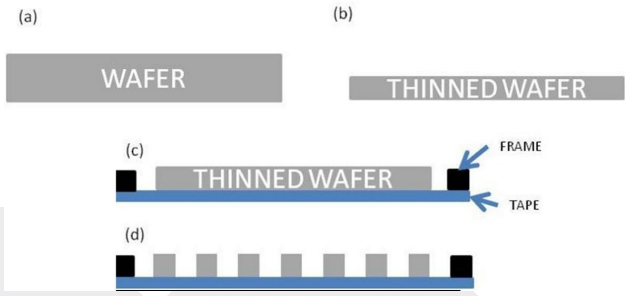

Fig 2 Schematic diagram illustrating Dicing After Grind

SPTS has successfully demonstrated plasma dicing after grind, overcoming the challenges of process control, tape damage and vacuum handling of framed wafers after die singulation, not encountered in dicing before grind.

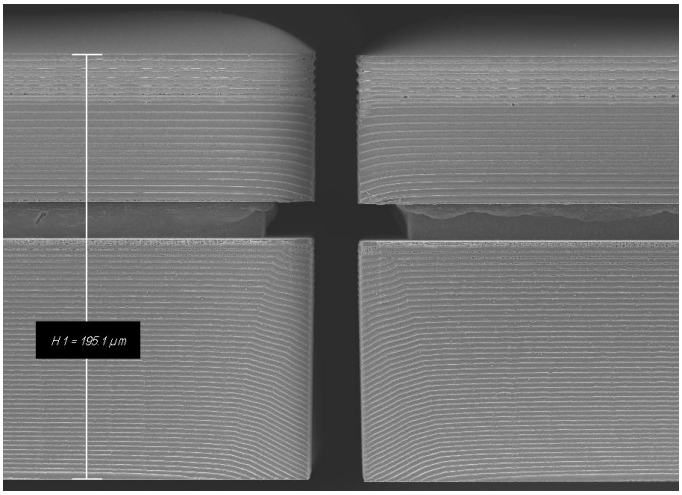

Fig. 4 Bonded wafer singulated by plasma dicing

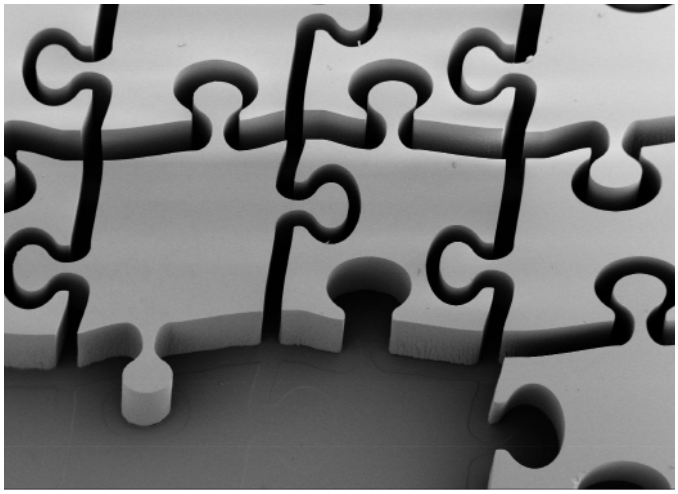

Fig. 5 Plasma diced test structure

Mosaic™ fxP Rapier System

Mosaic™ *f*xP systems are the production solution for plasma dicing.

Key Features:

- 4 process module facets for volume production settings
- Compatible with 296mm & 400mm frames
- Able to handle plastic and metal frames
- Frame contact end effectors to protect wafer & die
- Alignment of wafer (on frame) for etch process repeatability

Rapier-S Process Module

Based on the class leading SPTS Rapier plasma source for Si DRIE.

Key Features:

- Unique dual source design
- High Si etch rates for high wafer/die throughput
- No notching/undercut of die
- Sidewall scalloping control for application needs
- Complete substrate management & cooling
- Able to support widest range of tapes

Claritas™ End-Point Detection (EPD)

Claritas provides most sensitive OES EPD control for plasma etch to dicing tape

Key Features:

- Sensitive to <0.05% open areas
- Gives repeatable etch behaviour w2w/b2b
- Accounts for any variation in wafer thickness
- Maximizes throughput by minimizing overetch

Sentinel™ Wafer Protection

The Sentinel™ wafer monitoring system (patent-pending) has been developed by SPTS to ensure plasma dicing can be safely adopted

Key Features:

- Monitors silicon behaviour through etch
- Triggers alarm if there is a loss of cooling
- Prevents problems caused by poor taping
- Option to use as an additional end-point method

Fig. 6 Mosaic™ fxP Rapier-300S plasma dicing system

Demo Lab Capabilities

SPTS offers process demonstrations on customer sample wafers, in a dedicated plasma dicing lab in our UK headquarters. In addition to plasma dicing, we can also offer peripheral process steps including mounting on 296mm or 400mm frames, coating and laser grooving, post-dicing strip and clean and complementary metrology tools.

SPTS Technologies, a KLA company, designs, manufactures, sells, and supports etch, PVD, CVD and MVD® wafer processing solutions for the MEMS and sensors, advanced packaging, photonics, high speed RF, and power device markets. For more information, email enquiries@spts.com or visit www.spts.com