SPTS
A KLA Company

APPLICATION
BRIEF

Fan-Out WLP - PVD Processes

Introduction

Fan-Out WLP (FOWLP) technology is an enhancement of standard wafer-level packages (WLPs) developed to provide a solution for semiconductor devices requiring a higher degree of integration and a greater number of external contacts. It provides a smaller package footprint with higher input/output (I/O) along with improved thermal and electrical performance.

In conventional WLP schemes I/O terminals are located over the chip surface area. Using this method, there is a limitation to the number of I/O connections.

FOWLP takes individual die and embeds them in a low cost material such as epoxy mold compound (EMC) with space allocated between each die for additional I/O connection points – avoiding the use of relatively expensive Si real estate. Redistribution Layers (RDL) are formed using PVD seed deposition and subsequent electroplating/patterning to re-route I/O connections on the die to the mold region.

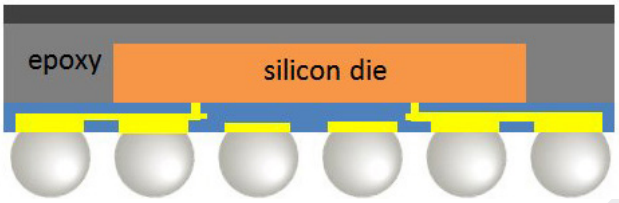

Fig 1 Schematic illustration of FOWLP

Mold compound is a cost-effective material for this application, but readily absorbs moisture when exposed to atmosphere. Outgassing during the PVD process sequence can have detrimental effects on package contact resistance (known as Rc or RVIA) so effective degas is essential. However, the material also has low thermal budget (TMAX typically <120°C) to prevent decomposition and excessive wafer warp. Consequently an effective degas requires long process times at low temperature. This significantly reduces system throughput for traditional single wafer-based degas systems, impacting CoO and capacity. Figure 2 shows how Rc for FOWLP test vehicle wafers improves with longer degas times.

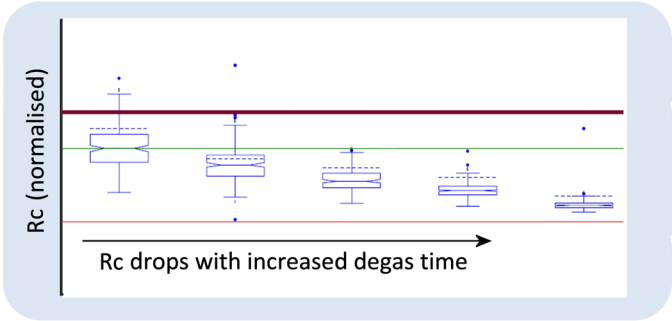

Fig 2 Benefit of increasing degas time - Reduced Rc

Multi-Wafer Degas

Improved Rc and Throughput

To eliminate the degas bottleneck SPTS offers a "Multi-Wafer Degas" solution (MWD) that enables a large number of wafers to be degassed in parallel before continuing to pre-clean and sputter deposition process modules without breaking vacuum. Wafers are dynamically pumped under clean, high vacuum conditions, with direct wafer heating to ensure efficient, effective heat transfer.

A Sigma® *f*xP PVD system configured with MWD will deliver throughputs >1.5x competitor systems based on single wafer degas processing technology. As materials emerge with lower thermal budgets, longer degas times can be employed with no impact on throughput. The module also offers potential to remove oven pre-bake steps prior to PVD from the FOWLP process flows. Conversely, competitor systems based on single wafer degas will get progressively slower (see Fig 3 overleaf).

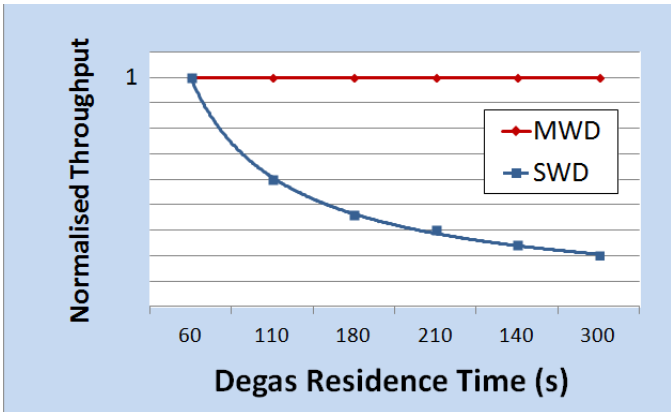

Fig 3 Throughput advantage of MWD versus single wafer degas increases with longer degas time

SE LTX Pre-Clean

Improved MWBC

With I/O counts increasing in FOWLP schemes the amount of exposed metal contacts on the wafer presents challenges for MWBC with ICP-based pre-clean chambers. Metallic contamination from the over-etch disrupts RF coupling through the ceramic chamber wall, leading to process stability issues.

The SE LTX pre-clean module is specifically designed to overcome this challenge. Specialized hardware prevents continuous build-up of metal on chamber walls while providing good adhesion for organic passivation materials sputtered onto the sidewalls as a by-product of the pre-clean process, resulting in a typical particle performance with > 5000 wafers MWBC.

Inspira™ PVD

Cost-effective Cu Seed

With degas and pre-clean stages completed the final stage of the PVD RDL process is the deposition of pre-plate seed layer. Typically Ti or TiW adhesion/barrier followed by Cu seed, this stage of the process requires relatively uniform, repeatable metal films over low topography. Inspira™ PVD technology designed specifically for BEOL processing with the emphasis on low CoO is used.

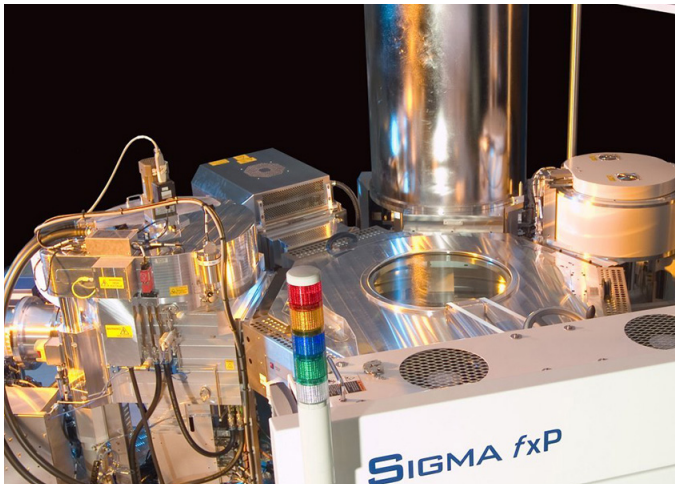

Fig 4 300mm Sigma® fxP with MWD

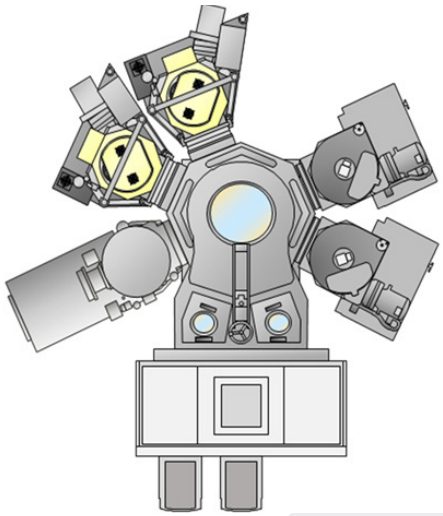

Fig 5 Plan view of Sigma® fxP with (clockwise) MWD, 2 SE LTX & 2 Inspira process modules

Cost Reduction Trends

Processing reconstituted wafers means wafer sizes are not necessarily limited to Si diameters and this presents opportunities for cost reduction. The Sigma® *f*xP PVD solution has been designed to run substrates up to 330 mm in diameter, giving a 20% increase in surface area for additional die to be processed in the same pass, reducing overall cost per die. Mold thickness can also be reduced, saving material cost. Wafer bows can increase as a result of either modification. Consequently the Sigma® *f*xP has been designed to accommodate wafers with up to 10 mm bow.

The combination of batch degas, high productivity pre-clean and Inspira hardware tailored for BEOL, results in Sigma® *f*xP being the most productive FOWLP PVD RDL system in the industry.

SPTS Technologies, a KLA company, designs, manufactures, sells, and supports etch, PVD, CVD and MVD® wafer processing solutions for the MEMS and sensors, advanced packaging, photonics, high speed RF, and power device markets. For more information, email enquiries@spts.com or visit www.spts.com