Fan-Out Wafer Level Packaging: Breakthrough advantages and surmountable challenges

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New wafer processing technologies overcome FOWLP's technical hurdles, paving the way for a new generation of ultra compact, high I/O electronic devices

Our ability to create ever-smaller electronic devices that maintain or surpass the performance of their physically larger predecessors – exemplified by today's wearables, smartphones and tablets – is dictated by many factors that extend well beyond Moore's Law, from the underlying embedded components to the ways in which they're packaged together. With regard to the latter, fan-out wafer level packaging (FOWLP) is quickly emerging as the new die and wafer level packaging technique of choice, and is widely anticipated to underpin the next generation of compact, high performance electronic devices.

Whereas with conventional flip-chip WLP schemes the I/O terminals are spread over the chip surface area, limiting the number of I/O connections, FOWLP embeds individual die in an epoxy mold compound (EMC) with space allocated between each die for additional I/O connection points, avoiding the use of more expensive silicon real estate to accommodate a higher I/O count. Redistribution layers (RDLs) are formed using physical vapor deposition (PVD) and subsequent electroplating and patterning to re-route I/O connections on the die to the mold compound regions on the periphery (**FIGURE 1**).

Leveraging FOWLP, semiconductor devices with thousands of I/O points can be seamlessly connected via finely-spaced lines as thin as two to five microns, maximizing interconnect density while enabling high bandwidth data transfer. Significant height and cost savings are achieved via the elimination of the substrate.

With FOWLP today we have the ability to embed heterogeneous devices including baseband

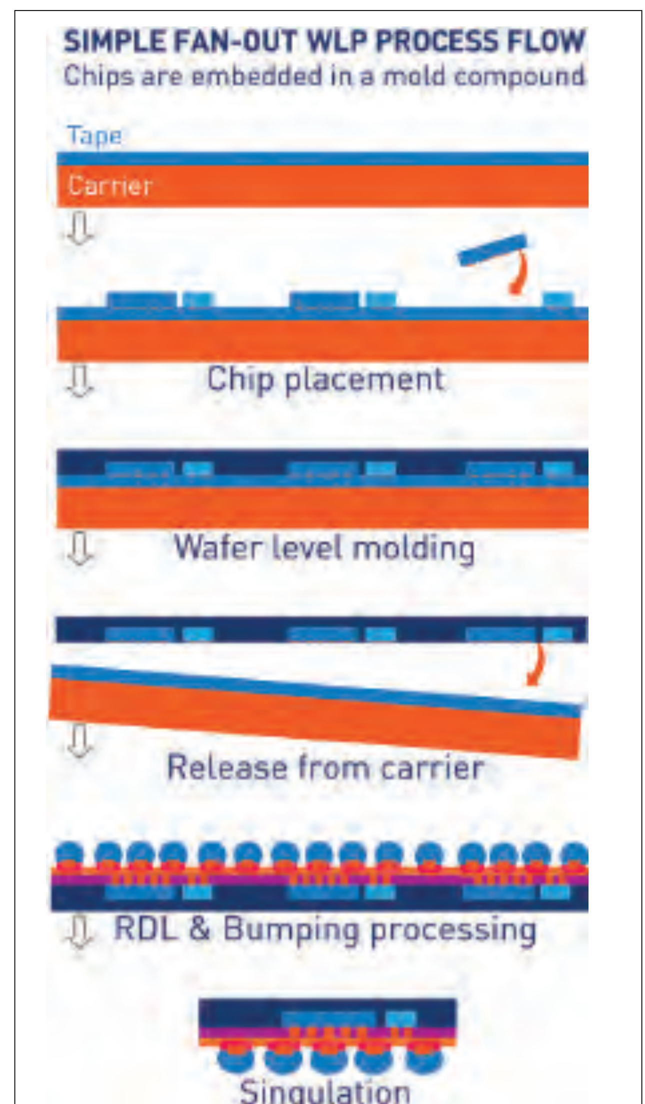

FIGURE 1. FOWLP process flow.

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processors, RF transceivers and power management ICs in these mold wafers, thereby enabling the latest generation of ultra-thin wearables and mobile wireless devices. With continued line and space reductions, FOWLP has the potential to accommodate higher performing devices including memory and application processors, positioning FOWLP to extend into new markets including automotive and medical applications and beyond.

Leading vendors implementing FOWLP today include Amkor, ASE, Freescale, NANIUM, STATS ChipPAC, and TSMC, with TSMC being the most high-profile vendor given its widely-reported contract win to produce A10 processors for Apple's iPhone 7 – a deal said to be attributable in part to TSMC's mature FOWLP-based InFO technology.

According to a report entitled "FO WLP Forecast update 09/2015" published by research firm Yole Développement in September 2015, the launch of TSMC's InFO format is expected to increase industry packaging revenues for FOWLP from $240M in 2015 to $2.4B in 2020. With a projected 54% CAGR, Yole expects FOWLP to be the fastest growing advanced packaging technology in the semiconductor industry.

Low heat, high speed processing

All fan-out wafers feature singulated die embedded in the EMC, with spin-on dielectrics surrounding the RDL. These materials present some unique challenges, including moisture absorption, excessive outgassing and a limited tolerance to elevated temperatures. If not dealt with properly, contamination at the metal deposition stage can compromise contact resistance.

Whereas conventional circuits built on silicon can withstand heat up to 400oC and can be degassed in under one minute, the EMC and dielectrics used in FOWLP have a heat tolerance closer to 120oC. Temperatures exceeding this low threshold can cause decomposition and excessive wafer warping. Degassing wafers at such low temperatures naturally takes a longer amount of time, and can drastically reduce the throughput of a conventional sputter system.

Multi-wafer degas (MWD) technology has emerged as a compelling solution to this problem, enabling up to 75 wafers to be degassed at 120oC in parallel before being individually transferred to subsequent pre-clean and sputter deposition, without breaking vacuum. With this approach, wafers are dynamically pumped under clean, high vacuum conditions, with radiation heat transfer warming wafers directly to temperatures within the operating budget for packaging applications.

Each wafer can spend up to 30 minutes inside the MWD, but because they're processed in parallel, a "dry" wafer is outputted for metal deposition every 60 to 90 seconds, at a rate of between 30 to 50 wafers per hour. This approach increases PVD system throughput by 2-3 times compared to a single wafer degas processing technology, and as materials emerge with even lower thermal budgets based on increased passivation thickness, longer degas times can be accommodated with no impact on throughput (**FIGURE 2**).

These benefits are not readily attainable, however, unless we can overcome the attendant warping challenges. Epoxy

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mold wafers can be warped after curing, and the size and shape of the warpage hinge on the different shapes, densities and placement of the embedded die. A FOWLP PVD system must therefore be able to minimize temperature-induced shape shifting, and accommodate wafers with up to a 10mm bow. The acceptable industry threshold for bowing is probably lower than 6mm, however, as it's not easy to make uniformly thick conductors on a substrate exhibiting 6mm+ warpage.

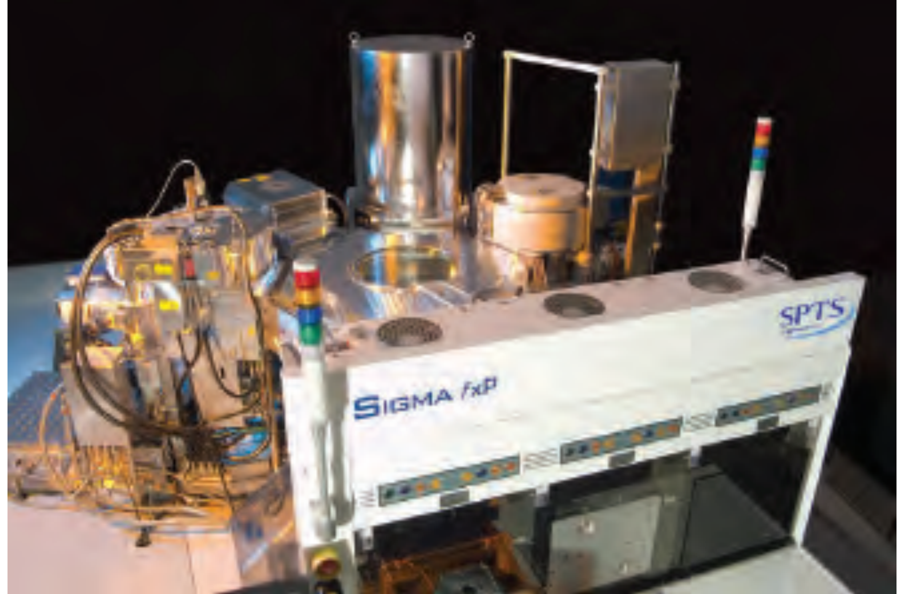

FIGURE 2. The Sigma® fxP PVD system with multi-wafer degas module from Orbotech-SPTS.

Utmost integrity

After successful degas, but prior to metal deposition, the FO wafer is pre-cleaned in a plasma etch module. This facilitates the removal of trace oxide layers from the contacts, but due to the composition of the organic dielectric surrounding the contacts, will result in carbon build-up on the chamber walls. This carbon does not adhere well to ceramic chamber surfaces, and if not carefully managed, can result in early particle failure.

New in-situ paste technologies allow these carbon deposits to better adhere to chamber surfaces during the pre-cleaning process, enabling preventative maintenance intervals that exceed 6,000 wafers. This approach can significantly improve productivity by reducing the frequency of dedicated wafer pastes, which typically require production to be paused every 10 to 20 wafers for chamber pasting when using conventional techniques.

The myriad benefits that FOWLP promises for the production of ultra compact, high I/O electronic devices far outweigh the aforementioned technical barriers to mainstream FOWLP adoption. With the ability to overcome the degassing, warping, and integrity challenges that can impede FOWLP implementations, electronics manufacturers can unlock the full potential of FOWLP while eliminating frictions affecting production speeds and yields. ◈