Plasma dicing: benefits and process considerations

Plasma dicing has gained acceptance within the semiconductor industry as a viable alternative to conventional singulation methods using saw blades or lasers, with significant adoption across a range of applications.

The technology is based on deep reactive ion etching (DRIE)—also known as the "Bosch Process"—a dry plasma etch process that has been in production use for over 20 years within the MEMS and 3D Packaging markets.

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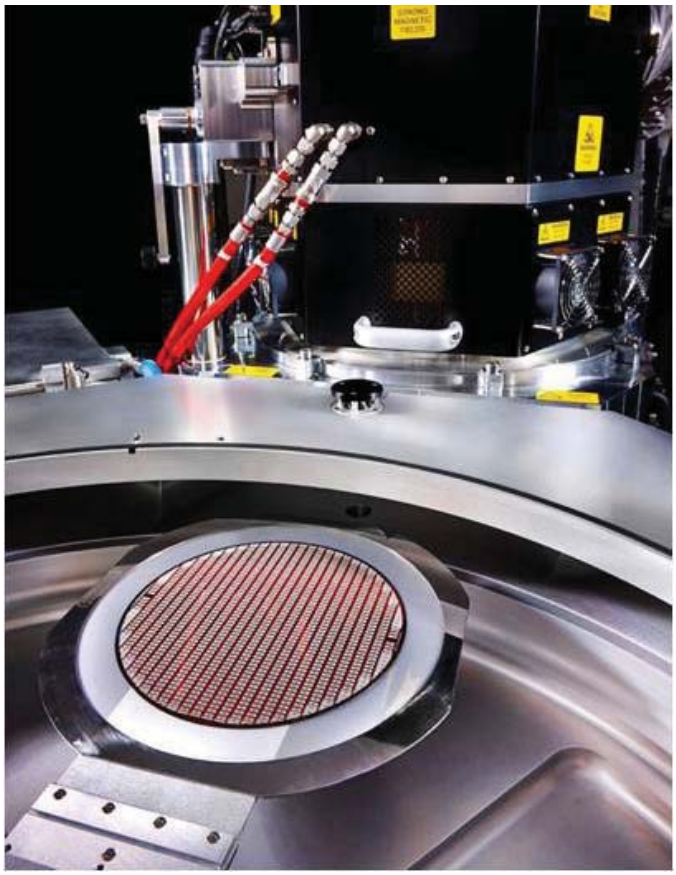
Etches narrow, deep trenches

DRIE, which can etch very narrow, deep vertical trenches, can be used to etch dicing lanes from <10µm to >100µm wide on wafer thicknesses from <50µm to full thickness to separate individual die.

Production-ready DRIE equipment for plasma dicing is available for wafers from 100mm to 300mm.

Plasma dicing offers considerable benefits for die singulation, with opportunities to achieve increased throughput and die count on the silicon area; flexibility for die layout and design; and perhaps most important of all—improved die quality and strength.



This plasma dicing system uses DRIE-based technology. (Orbotech)

As such, it's well positioned to become the benchmark technology for fabs seeking to increase throughputs and yields for small or thinned fragile die.

Etching before or after grind

The plasma etch process can be carried out *before grind*, where deep dicing lanes are etched into the wafer and the die are singulated by a final backside grind operation, or *after grind*, where DRIE is used to etch through thinned wafers mounted on taped frames.

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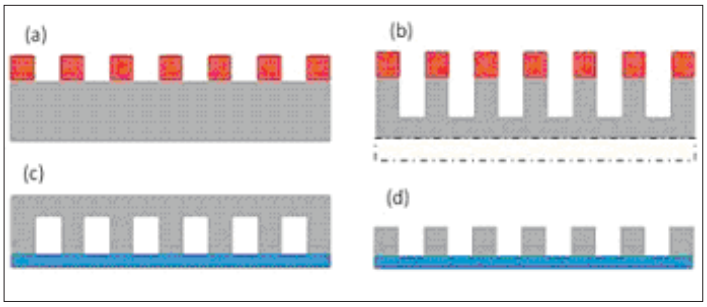
Dicing before grinding (DBG)

In the DBG approach, die are defined by partially etching the front side of a masked wafer, typically to etch depths of 100µm to 200µm.

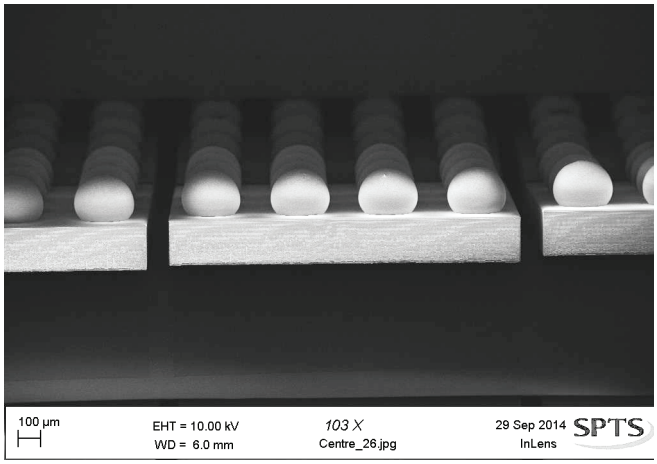
The wafer is then attached face-down to a dicing frame, and the backside of the wafer is ground away until the die is singulated.

Exceptional control needed

This method, although relatively straightforward, requires exceptional control of etch-depth uniformity to ensure the subsequent grind operation does not leave die unsingulated or cause over-grinds that result in die loss.



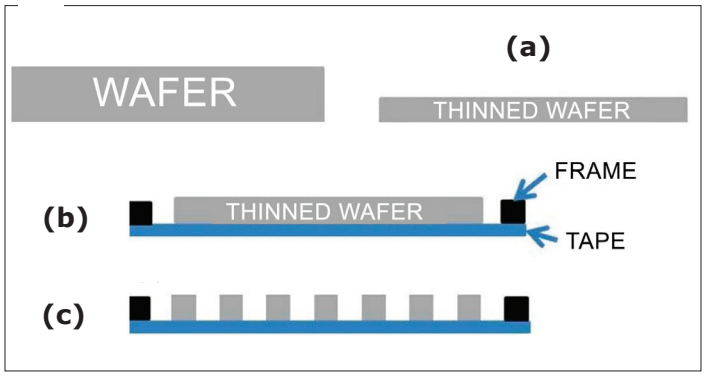
In the graphic above representing dicing before grinding, image a. is patterning; b. is a front-side partial cut; c. is grinding and d. shows the final singulation. SEM below shows DBG.



DBG using well-established DRIE processing has been successfully employed in volume production for many years.

Dicing after grinding (DAG)

In DAG (below), device wafers are thinned (a), then taped onto frames (b). The die are then singulated by etching through the complete silicon thickness, to the tape (c). This is a "drop-in" replacement for conventional mechanical saw processing.



DAG, however, is more challenging as the etch continues until the tape is exposed, at which point the insulating tape can act in a way similar to the insulating layer when etching slicon-on-insulator (SOI) wafers.

Electrical charge build-up on the insulator tends to deflect ions into the sidewall at the interface of the silicon and tape/insulator and cause damage or "notching" of the silicon at the interface.

Avoid notching

Care must be taken to avoid this notching of the die due to the potential side effects, while preventing any damage to the tape, which has to endure prolonged exposure to the process after singulation begins.

As die sizes shrink, allowing more die to be patterned onto wafers, the number of dicing lanes increases. Consequently, the dic-

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ing time for a serial process like conventional mechanical saw or laser dicing becomes significantly longer.

Parallell process

Because the plasma etch process is a parallel process, with all dicing lanes etched simultaneously, the throughput of plasma dicing is largely governed by the etch rate and wafer thickness—not by the number of dicing lanes or die per wafer.

Also, with the industry generally driven toward thinner die, mechanical sawing and laser dicing become more difficult and cause decreases in throughput as feed speeds need to be reduced to prevent damaging these fragile devices.

Conversely, for plasma dicing, thinner wafers are quicker to etch through, which inceases throughput, while preserving the physical integrity of the die.

Increased die counts

When using a conventional dicing saw, the lane width is determined by the width of the saw and the various tolerances used to account for accuracy and damage limitation.

Plasma dicing lanes are not restricted in the same way and therefore can be much narrower than the width of a blade, freeing valuable silicon real-estate for more die per wafer.

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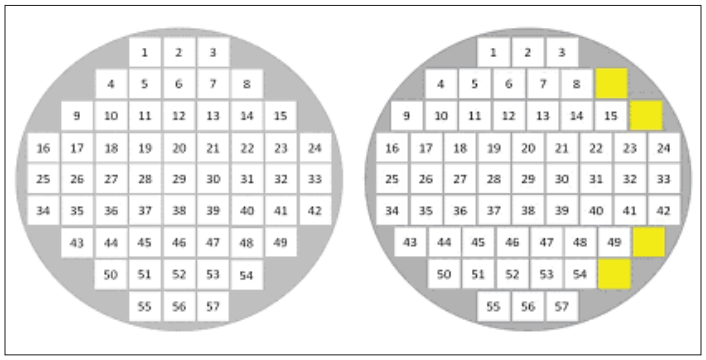
For smaller die—RFID chips for example (at ~0.04mm^2)—this saved real-estate can yield a potential increase of 80 percent more die per wafer.

Increase in die per wafer

Even disregarding the possibility of reducing the width of the dicing lanes, a significant increase in die per wafer can be achieved when using plasma dicing because the wafer layout is not constrained by the need to have linear dicing paths.

Plasma dicing can offer device designers much greater flexibility with regard to fundamental die shape/size, removing guard rings and positioning of die/test groups to make better use of the wafer area.

A simple example, illustrated below, shows how even for large die, where reduction in lane width is less significant, the ability to shift the die positions may increase the number of die per wafer.



Increasing die count by using "non-linear" dicing lanes allows more efficient use of silicon real estate.

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Increased yields

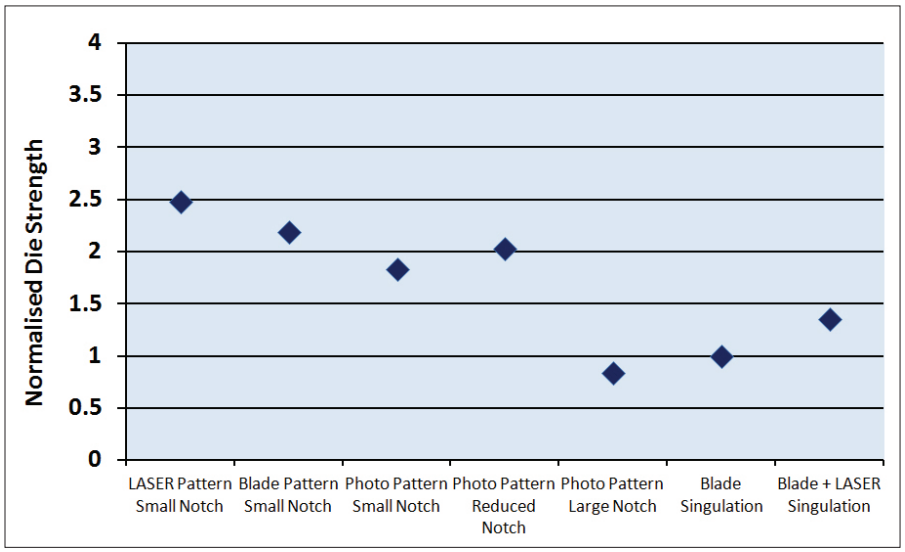
In mechanical dicing, especially for small, thin die or when using high feed speeds, chipping at the edge of the die may be an issue.

In laser dicing, there is also heat damage to account for, which becomes more significant for smaller die.

Plasma dicing is non-damaging and produces die with significantly improved strength compared to traditional methods, a valuable attribute as form-factor roadmaps push die thicknesses below 50µm.

Attractive for fragile devices

Plasma dicing is also attractive for fragile devices such as MEMS, since there are no physical forces to vibrate the wafer.



This figure shows die strength comparison between singulation techniques with varying patterning methods.

The keys to improving the strength of a die is to reduce damage at the die edges and to minimize notching at the Si-to-tape interface.

Two patented technologies, already well-established and proven in SOI MEMS applications, can be employed to prevent damage to the silicon and the tape during plasma dicing.

First, a proprietary end-pointing technology [2] can accurately monitor the progress of the etch front and trigger a change in recipe conditions when the tape is exposed.

"Bias Pulsing"

Patented "bias pulsing" [3] can then be used during the final stage of die singulation to control the final stages of the etch, preventing any lateral underetching (notching) of the die.

The graph (at left) shows how the strength of plasma-diced die with "small" or optimized (reduced) notching is typically twice that of a blade or blade/laser approach.

Plasma dicing with no control of the notching, however, will severely compromise die strength.

Challenges

Introducing plasma dicing into an existing process flow can be less than straightforward.

One of the main obstacles is that DRIE will not etch any metal layers in the dicing lanes. This can be "designed out" for new device layouts, but for existing products it may be necessary to remove the metal layers earlier in the process flow, or use either lasers or mechanical saws to "pre-define" the dicing lanes.

Using this method is more typically valid for larger die, which will be less affected by the

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obvious throughput impediments of the definition step.

Using existing layers

Other methods for defining the dicing lane include standard photolithography and use of existing layers, extended to allow for erosion of the material during etching. This latter method can be described as maskless.

Recent work [4] shows that a significant strength/yield increase can still be achieved for a combination of laser or blade pre-definition and plasma dicing.

The graph (page 18) also emphasizes the importance of plasma processing control, illustrating how plasma dicing—even defined by photolithography—may, in fact, reduce die strength if the process control is poor and a large notch is allowed to form.

Plasma dicing can offer significant advantages over conventional dicing methods, but without good process control these benefits can be negated by undesirable damage to the die.

Summary

Designing-in plasma dicing from the outset of a device life cycle is perhaps the only way to realize all the benefits that plasma dicing can provide.

Novel approaches within current device process flows, however, have proven that plasma dicing can be immediately adopted and significant advantages can be realized—namely improved device quality.

Plasma dicing after grind is at the early stages of adoption for volume production, however, the trend toward thinner, smaller die distinguishes it as an increasingly attractive alternative to mechanical saw or laser solutions.

References

1. *Thin Wafer Processing and Dicing Equipment Market report,* Yole Développement, (May 2016)
2. U.S. Patent No. 9,159,599, "Apparatus for chemically etching a workpiece."
3. U.S. Patent No. 6,187,685 , "Method and apparatus for etching a substrate"
4. R. Barnett, D. Thomas, O. Ansell, et al., "Improving Device Yields and Throughput using Plasma Dicing," Proc. IWLPC, (2015).

An analyst's perspective

Amandine Pizzagalli, Technology & Market Analyst from Yole Développement comments: "Dicing technology today is applied in numerous device applications such as logic and memory; MEMS & power electronics devices; RFID components; and CMOS image sensors. Driven by the rising demand for thinner wafers and stronger die, dicing technology is evolving and ready for innovative equipment. The promising plasma dicing approach will grow in the semiconductor sector.

Mr. Barnett is etch product manager at SPTS, an Orbotech company, with 20 years' experience in the semiconductor and electronics manufacturing industries. Prior to his current role, he worked in product management and as a process engineer at both Aviza and Surface Technology Systems (STS), prior to their merger to form SPTS.

He earned a Bachelor's degree in engineering for material engineering and electronics at the University of Nottingham, England.