SPTS
A KLA Company

APPLICATION
BRIEF

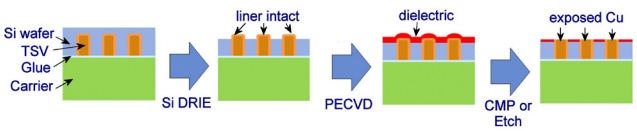
Via Reveal Processing

Introduction

Through silicon vias (TSVs) are being implemented in place of traditional scaling for increasing device performance and reducing form factor. SPTS plasma etch and deposition are used for initially creating and lining these interconnect vias.

In addition, SPTS processes can also be used for post-TSV steps, to prepare the die for connection to other parts of the device.

Via Reveal Process

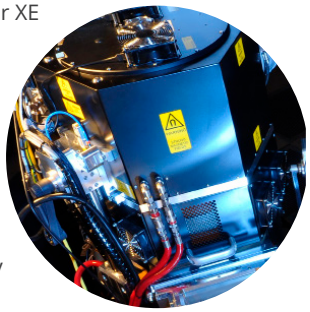


Schematic diagram illlustrating via reveal processing

After completion of the front-side wafer processing (typically via middle) the wafer is temporarily bonded, face down, onto a carrier which can be glass or another silicon wafer. The active silicon is then ground typically to within 5-10 µm of the TSV nodes. After grinding the silicon is dry etched in a process that 'reveals' the vias to a step height of around 5 µm.

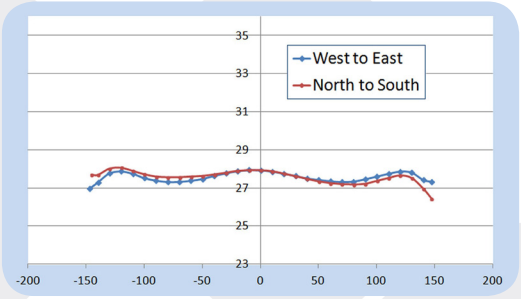
After silicon etching the vias are passivated using a dielectric stack and then CMP'd (chemically mechanically polished) to expose the copper ready for RDL (redistribution layer) metallization.

Why Use SPTS?



- 2 to 3 times productivity gain with Rapier XE
  - Etch rate ~9µm/min
  - Non-uniformity <±3%
  - Low roughness
- ReVia® - unique end-pointing technique to monitor via reveal
  - Low via density <0.01%
  - Low reveal height ~1µm successfully endpointed
- Silicon etch is highly selective to oxide liner - prevents exposing the copper metal
- Dual plasma source with multi-mode operation - allows for uniformity tuning that can compensate for incoming wafer thickness variations
- Stable oxide and nitride passivation films can be deposited at low temperature (<180°C) with low stress and excellent mechanical/electrical properties
- Multi-wafer degas option to maintain film quality with increased throughput
- Etch and deposition modules can be integrated to single Versalis® *f*xP cluster platform to reduce cost of ownership for product development

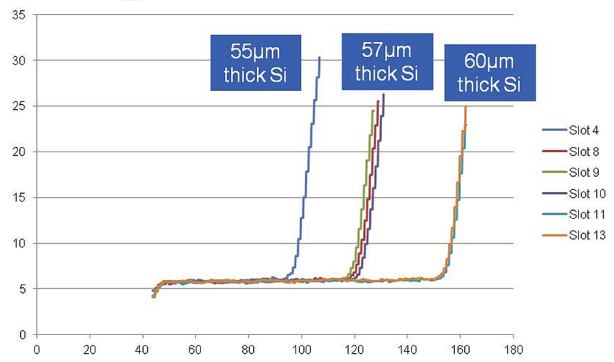
Etch Uniformity



27µm etch depth, etch rate 9.05µm/min, uniformity ±1.79%

ReVia® Endpoint System

SPTS offers a patent-protected endpoint system which enables in-situ monitoring of the reveal process, eliminating yield losses due to over-processing and costs due to manual post-processing inspection, and potential reprocessing. ReVia™ has successfully endpointed processes for extremely low via densities <0.01% and very low reveal heights ~1µm. Lower reveal heights decrease production costs by reducing etch times and subsequent passivation/CMP requirements.



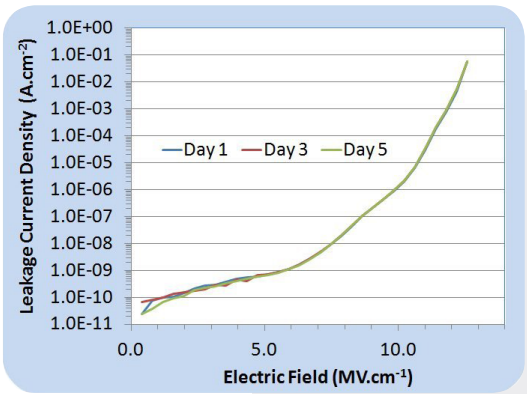
ReVia™ endpoint data for reveal height of 1µm (Courtesy of imec)

Dielectric Deposition

SPTS PECVD processing deposits thick, high quality SiN/SiO film stacks which provide mechanical stability to the revealed vias with good adhesion to withstand the subsequent CMP processing. The films must exhibit a low leakage current ensuring good electrical isolation between the silicon and overlying metal conductor, with a high breakdown voltage for reliability.

The stress of the stack must typically be low and compressive although some stress tuning capability is desirable to control wafer bow.

SPTS PECVD films have demonstrated excellent stability over time, which is important to ensure device reliability.

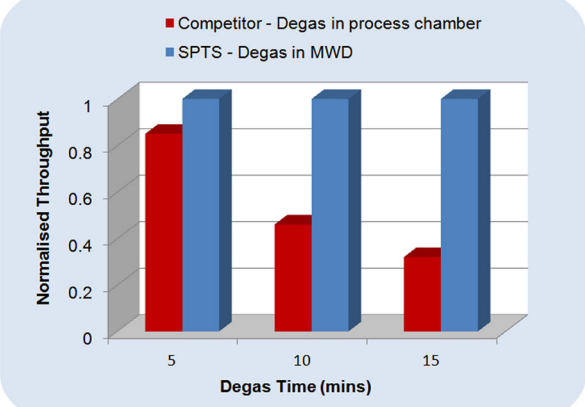


Stability of leakage current density over 5 days

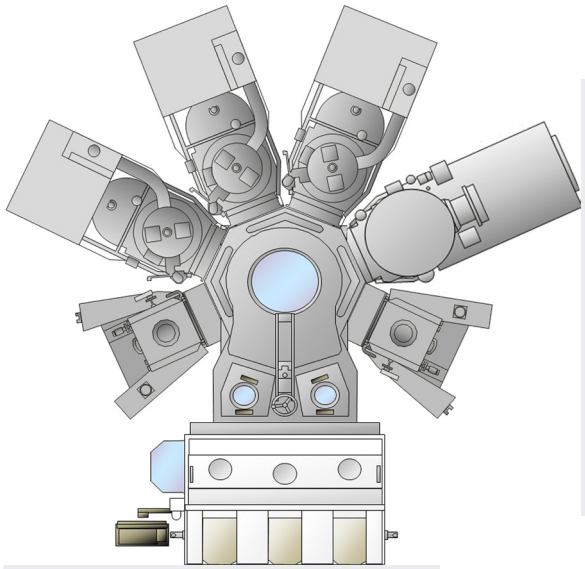
Multi-Wafer Degas Module

Dielectric passivation – typically a SiN/SiO stack – must be deposited at <~175°C to maintain the integrity of the temporary bond. The bonding adhesive will also out-gas inside the PECVD vacuum module, potentially disrupting the plasma and the quality of the growing film. Therefore, in order to maintain the film quality it is necessary to degas the bonded wafer prior to deposition. After degassing the wafer must not be exposed to atmosphere, otherwise the adhesive will begin to re-absorb moisture.

At lower temperature, the degassing process can take a long time which significantly reduces throughput. SPTS offers a unique solution which allows in-situ batch degassing of up to 75 wafers for long degas times without affecting throughput.



Throughput benefits of multi-wafer degas compared to single wafer degas



Layout of a Versalis® fxP with etch, deposition and multi-wafer degas modules for fully integrated via reveal processing

SPTS Technologies, A KLA Company, designs, manufactures, sells, and supports etch, PVD, CVD and MVD® wafer processing solutions for the MEMS, advanced packaging, LED, high speed RF on GaAs, and power management device markets. For more information about SPTS Technologies, email enquiries@spts.com or visit www.spts.com

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