SPTS
A KLA Company

APPLICATION
BRIEF

WLP of MEMS

Introduction

Micro electro mechanical systems (MEMS) devices, also known as micromachines, are typically fragile, often containing moving parts that can be damaged during dicing. Wafer level packaging (WLP) prior to wafer dicing can provide protection from particles and dicing slurry, while significantly reducing form factor and reducing the overall die cost.

Increasingly, many MEMS devices, such as microsensors, require a vacuum or controlled atmosphere for operation. This could be used to control parameters such as the Q-factor (amount of damping), or to provide a reference vacuum for pressure sensors, or to reduce absorption in infrared sensors and improve sensitivity and resolution. Two such examples of wafer level packaging are silicon capping and thin film encapsulation, each providing benefits for specific packaging applications.

Silicon Capping

One common method of packaging micromachined devices is to bond a silicon cap wafer to the device wafer. This can be used for multiple sensors on the same die, utilizes metal- eutectic bonding and requires less bonding area than traditional glass frit capping. Through-silicon vias (TSVs) can be used instead of I/O pads – further reducing form factor size.

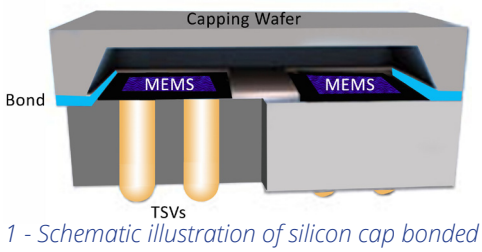


Fig 1 - Schematic illustration of silicon cap bonded to device wafer

Thin Film Encapsulation

A lower cost and simpler packaging alternative is thin film encapsulation. By eliminating the need for sealing/bonding and a capping wafer, thin film encapsulation is, for some MEMS designs, the simplest and lowest cost packaging alternative.

The technique uses a double sacrificial layer (normally silicon or silicon oxide) which supports the MEMS structure and defines a space above the structure while a cap layer is deposited over the device layer (Fig.s 2 & 3).

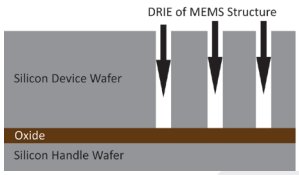


Fig 2 - MEMS etch

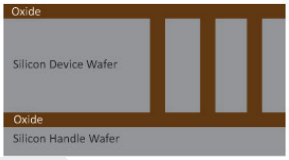


Fig 3 - Deposition

Holes in the capping layer allow an etchant (e.g vapor HF or XeF_2) to remove the sacrificial layer and "release" the moving MEMS structure (see Fig.s 4 & 5).

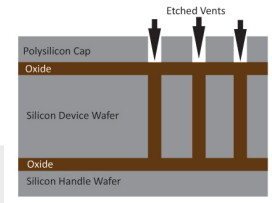


Fig 4 - Vent hole etch

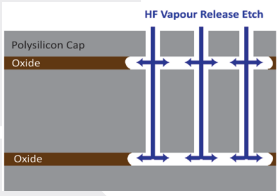


Fig 5 - MEMS release

These holes must then be closed by depositing a final sealing layer (Fig. 6). Typical sealing materials include epi- or LPCVD PolySi , PECVD SiOx or SiNy or metals such as aluminium.

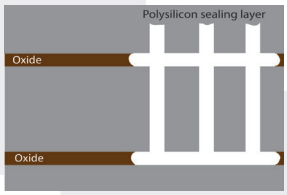
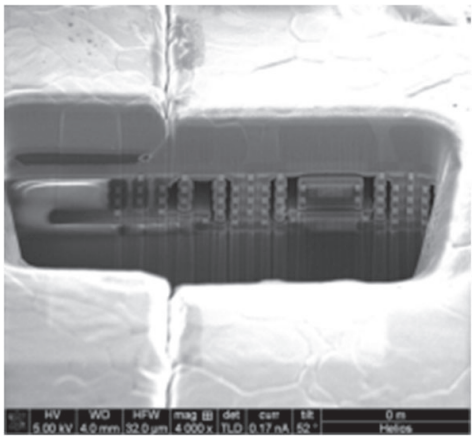
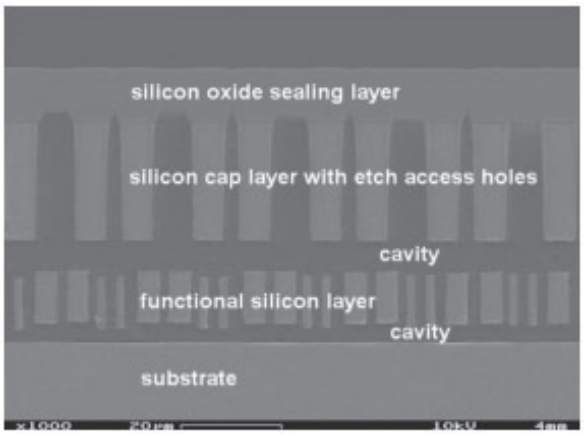


Fig 6 - Sealing

Examples of WLP of MEMS using Thin Film Encapsulation



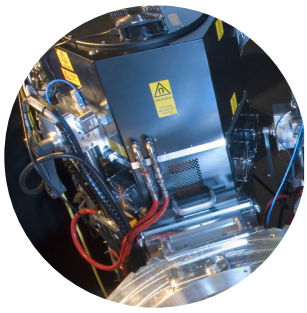
Encapsulated CMOS MEMS device released using HF vapor (Image courtesy of Baolab Microsystems)



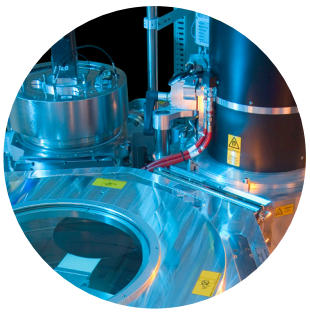
Wafer level encapsulation of MEMS accelerometer

Ideally, the device package should be sealed without removing the wafer from vacuum, to avoid yield or performance loss from unwanted absorption of contaminating gases or moisture.

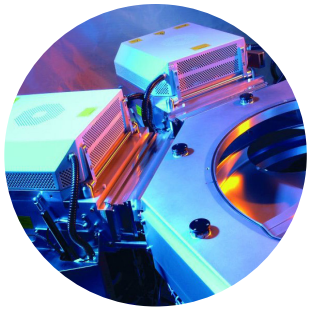
Different MEMS devices require different cavity pressures, and the required pressure/gas composition can be tailored prior to sealing. Stress, temperature and vacuum requirements will determine optimum sealing material.



Omega® Rapier for deep silicon etch



Versalis® with PVD and DRIE modules



Delta™ fxP PECVD system

Xactix® CVE modules for vapor XeF_2 etch

Why use SPTS?

- Market-leading DRIE etch processes to define MEMS structures and vent holes, with high etch rates, low feature tilt and unique Claritas™ end-point system.
- Low temperature PECVD compatible with temperature-sensitive MEMS devices
- HF or XeF_2 vapor etch processes can be integrated onto production-proven cluster systems
- Versalis® *fx*P enables integration of different single-wafer processes into a single cluster tool to reduce cost of ownership
- LPCVD batch processing for cost-effective deposition of thick polysilicon layers, and dielectrics where low temperature is not a requirement.

For more information about our wafer level packaging solutions, please email enquiries@spts.com.

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